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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,197	12/15/2003	Chin-Cheng Chien	025796-00013	4786

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EXAMINER

DUONG, KHANH B

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/734,197	<b>Applicant(s)</b> CHIEN ET AL.	
	<b>Examiner</b> Khanh B. Duong	<b>Art Unit</b> 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 18 October 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☐ Claim(s) \_\_\_\_\_ is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 18, 2005 has been entered.

### *Response to Amendment*

This Office Action is in response to the amendment filed October 18, 2005.

Accordingly, claims 1 and 11 were amended.

Currently, claims 1-20 remain pending.

### *Response to Arguments*

Applicant's arguments with respect to the amended claims have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

**Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

Claim 1 recites the limitation "said polysilicon gate electrode" in lines 8 to 9. There is insufficient antecedent basis for this limitation in the claim.

\*\*\* Other claims are rejected as depending on the rejected base claim.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

**Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon (US 2003/0025163 A1) in view of Murthy et al. (US 6,541,343) and Wieczorek et al. (US 6,274,894).**

Kwon discloses in Figs. 6-11 a method of forming a semiconductor device using selective epitaxial growth, comprising: providing a semiconductor substrate 200 with a first conductivity; forming a plurality of isolation regions 202 on said semiconductor substrate 200; sequentially forming a gate dielectric layer 204 and a gate electrode 206 on said semiconductor substrate 200 between each pair of said isolation regions 202; forming a lightly doped drain region 212 with a second conductivity opposite to said first conductivity in said semiconductor substrate 200 between said gate electrode 206 and each said isolation region 202; forming a first (offset) spacer

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214a around said gate dielectric layer 204 and said gate electrode 206; forming a source/drain region 226 with said second conductivity beside said lightly doped drain region 212 in said semiconductor substrate 100; performing a baking process with hydrogen ambient gas at a temperature of 900°C prior to said selective epitaxial growth process; performing a selective epitaxial growth process to form a semiconductor layer 224 on said gate electrode 206, said source and drain regions 226; forming a metal layer 228 on said semiconductor layer 224; and performing a salicide process to form a silicide layer 224a on said gate electrode 206, said source and drain regions 226.

Re claims 1-20, Kwon fails to disclose: performing a dry etching process with a carbon-free plasma source to remove a portion of said semiconductor substrate; performing the baking process with hydrogen ambient gas at a temperature of 750°C; and forming a pocket region by angle implanting said semiconductor substrate with said first conductivity on the interface of said lightly doped drain region and said semiconductor substrate.

Murthy suggests in FIG. 2 to 3 performing a dry etching process with a carbon-free plasma source (SF<sub>6</sub> diluted with ambient gas comprising He) to remove a portion of said semiconductor substrate 201 for the purpose of cleaning the surface of the substrate 201 prior to forming a silicon epitaxial layer 216 [see col. 5, lines 18-32 and 55-60]. Murthy further discloses performing the dry etching process at a pressure between 200 to 300 mTorr and a power between 25 to 100 Watts [see col. 5, lines 23-32]. However, Murthy fails to suggest forming a pocket region by angle implanting said semiconductor substrate with said first conductivity on the interface of said lightly doped drain region and said semiconductor substrate.

Wieczorek et al. ("Wieczorek") suggests in FIG. 4 forming a pocket ("halo") region 36 by angle implanting a semiconductor substrate 10 with a first conductivity on the interface of a lightly doped drain region 18 and said semiconductor substrate 10 for the purpose of directing the implanted impurities below the edges of the gate electrode 14 [see col. 4, lines 43-47].

Since Kwon, Murthy and Wieczorek are all from the same field of endeavor, the purposes disclosed by Murthy and Wieczorek would have been recognized in the pertinent prior art of Kwon.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the dry etching process of Murthy to the process of Kwon because of the desirability to provide the substrate with a clean surface free of contaminants prior to growing the epitaxial silicon layer. In addition, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the angled pocket implant process of Wieczorek to the process of Kwon because of the desirability to direct the implanted impurities below the edges of the gate electrode.

Re further claims 4-10 and 14-18, Kwon and Murthy fail to disclose the specific ranges of process parameters for temperature, volume ratio, pressure, power, time and thickness as claimed.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to optimize and select specific ranges of process parameters as claimed. The selection of parameters such as energy, power, concentration, temperature, time, depth, thickness, etc., would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in

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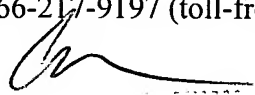
temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce new and unexpected result which is different in kind and not merely degree from results of prior art ... such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality ... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In re Aller*, 105 USPQ 233, 235 (CCPA 1955). See also MPEP 2144.05.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on Monday - Thursday (9:00 AM - 6:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
KBD  
AMIR ZARABIAN